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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/653,243	09/03/2003	Woo-Hyun Kim	041993-5232	2820

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EXAMINER

VU, PHU

ART UNIT	PAPER NUMBER
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2871

DATE MAILED: 01/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/653,243

Applicant(s)

KIM, WOO-HYUN

Examiner

Phu Vu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Kim et. al US Patent 6,335,776 or its priority documents KR-98-19997 and KR-99-00542 [Note: in the reference auxiliary electrode and side electrode are used interchangeably]. Kim teaches a liquid crystal display panel, comprising: a plurality of gate lines arranged along a first direction on a first substrate, (see claim 1), a plurality of data lines arranged along a second direction on the first substrate to cross the gate (see claim 1) lines to define a plurality of unit pixels, an insulating layer disposed over the gate and data lines, a common electrode disposed on a second substrate (see claim 1) opposite to the first substrate a plurality of pixel electrodes, each pixel electrode provided in each of the unit pixels partitioned by the gate line and the data line (see claim 1) and a plurality of side electrodes overlapping the data lines (see claim 8 which is a dependent claim of claim 1) and regarding the limitation wherein the insulating layer is provided between the side electrode and the data lines (see claim 1 which is dependent on claim 7) the reference teaches the a passivation layer insulating the pixel and side electrodes insulated from all other lines and electrodes which includes the data lines.

Regarding claim 2 the reference teaches the panel according to claim 1, further comprising a thin film transistor provided in the unit pixel (see figures 2A-17C lower left area).

Regarding claim 3, the reference teaches the pixel electrode and the side electrode are made of a same material (see claims 4 & 5).

Regarding claim 4, wherein the common electrode and the side electrodes comprise transparent conductive material films. The reference teaches side electrodes and common electrodes made of ITO, which is used in construction of transparent conductive films. Therefore this limitation is inherent.

Regarding claim 5, the reference teaches a plurality of pixels formed by intersection of the gate and data lines (see). Since multiple pixels are formed and each has a pair of side electrodes than side electrodes will be found between a pair of adjacent unit pixels.

Regarding claims 6 and 7, the reference teaches a panel wherein the insulating layer includes an organic material film (see column 7 lines 27-30) and the insulating layer including benzocyclobutene (BCB) (see column 7 lines 27-30).

Regarding claim 8 the reference teaches overlap between the gate line and side electrodes (see column 9 lines 30-33) and the limitation of an insulator between them also taught by the reference because it teaches a passivation layer insulating the side electrode and pixel electrode from all other electrodes and bus lines (see abstract).

The panel according to claim 1, wherein the pixel electrode is divided into a first region and a second region and the first and second regions are electrically interconnected by a connection region.

Regarding claim 10 the reference teaches liquid crystal display panel, comprising a plurality of gate lines formed on a first substrate (column 5 line 23), a first insulating layer (figure 20A element 35) and an active layer (20A element 5) formed on the first substrate, a plurality of data lines (fig. 20 element 13) formed on a surface of the active layer, a second insulating layer formed on another surface (20A element 37) of the active layer upon which the data lines are formed, a plurality of side electrodes (20A element 15) formed on a surface of the second insulating layer to overlap the data lines (see column 7 lines 18-20), and a plurality of pixel electrodes formed on surfaces of the second insulating layer separated from the side electrodes (fig. 20A element 13).

Regarding claim 11, the first insulating layer is a gate-insulating layer (figure 20A element 35) separating a gate electrode (figure 20 element) from the active layer (figure 20 element 5).

Regarding claim 12 the reference teaches the second insulating layer includes an organic material layer (see column 7 lines 27-30).

Regarding claim 13, the reference teaches the panel further comprising: a second substrate bonded to the first substrate (figure 20A element 33) a liquid crystal material layer formed between the first and second substrates, a black matrix (figure 20A element 20A) formed on a surface of the second substrate aligned to the gate lines

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and the data lines, a color filter layer (figure 20A 23) formed on the second substrate aligned with the unit pixel, and a common electrode (figure 20 element 17) formed on another surface of the second substrate upon which the black matrix and the color filter layer are formed, and an electric field partition formed (distortions column 5 lines 35-38) on the second substrate. Also the reference shows prior art figures 1A and 1B element 19 showing a slit to distort the electric field (electric field partions) (see column 1 line 41).

Regarding claim 14 the reference teaches a display further comprising a liquid crystal material layer formed between the first and second substrates (see abstract).

Regarding claim 15, the reference teaches the liquid crystal material layer has negative dielectric anisotropy (see column 4 lines 62-63).

Regarding claim 18, the reference teaches a gap between the pixel electrode (see figure 20A element 19) and the side electrodes (see figure 20A element 15) which is considered be to a partition on the first substrate since the applicant discloses slits between electrodes forming partitions. Therefore this limitation is considered inherent.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim as applied to claim 1 above, and further in view of Baek US Publication No. 2002/0140892. Kim discloses all the limitations of the of claim 9 except, a pixel electrode divided into a first region and second region and these regions electrically connect. Beck discloses a multi-domain liquid crystal display where the pixel electrodes are split and the portions are electrically connect by a connecting member (see figure 1A element 94) to provide a display with an enhanced viewing angle (see [0002]). Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to add a pixel divided into portions that are electrically connected to one another to improve viewing angle.

Claim 16 and 19 rejected under 35 U.S.C. 103(a) as being unpatentable over Kim US Patent 6,335,776 as applied to claim 13 above, and further in view of Kim US Publication No 2001/0019388 (secondary reference). Kim (primary reference) teaches all the limitations of claim 16 except a the electric the electric field partition being a rib formed on a surface of the common electrode. Kim (secondary reference) discloses a rib (figs 2A-5B element 53) formed on a surface of the common electrode to form a plurality of domains thereby enhancing viewing angle (see [0011]). Therefore, at the time of the invention, it would have been obvious to one or ordinary skill in the art to form a rib on the surface of the common electrode to enhance the viewing angle.

Regarding claim 19, the primary reference discloses a method for fabricating a liquid crystal display panel, comprising: forming a plurality of gate lines, a plurality of data lines, and a plurality of thin film transistors on a first substrate forming a

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passivation layer on a surface of the first substrate upon which the gate lines, the data lines, and the thin film transistors are formed; forming a transparent conductive material on a surface of the passivation layer (column 5 lines 45-50).

The primary reference also teaches forming a plurality of side electrodes overlapping the data lines (see column 7 lines 18-20) by patterning the transparent conductive material (column 5 lines 61 and 62-63 ITO is the transparent conductive material) forming a plurality of pixel electrodes separated from the side electrodes by patterning the transparent conductive material (column 5 lines 62-63), forming a black matrix (element 25), a color filter (element 23), and a common electrode (element 17) on a second substrate (see figure 20A) bonding the first and second substrates together aligning the pixel electrodes to the common electrode; and forming a liquid crystal material layer between the bonded first and second substrates (see column 5 line 45 – column 6 line 2). The only limitation not disclosed by the reference is an electric field partition formed on the second substrate. Therefore the rejection follows that of claim 16. Kim (secondary reference) discloses a rib (figs 2A-5B element 53) formed on a surface of the common electrode to form a plurality of domains thereby enhancing viewing angle (see [0011]). Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to form a rib on the surface of the common electrode to enhance the viewing angle.

Regarding claim 20, ITO as use of a transparent conductive film has been shown (see rejection of claim 19).

Regarding claim 21, the primary reference has shown that the passivation layer (see figure 20A element 37) has been etched to expose part of the drain electrode (see figure 20A element 9).

Regarding claim 22, a rib surface has been shown thus the rejection follows that of claims 16 and 19 (see rejection of claim 16 and 19).

Regarding claim 23, forming a slit is shown as prior art disclosed by the primary reference (see figure 2 element 36). The reference does not disclosed that it is formed by etching however etching is a well-known technique used to pattern electrodes see US Patent 23548751.

Regarding claim 24, simultaneous formation of the electrodes is taught by the primary reference (see column 5 lines 63-65).

Claims 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim US Patent 6,335,776 as applied to claim 13 above, and further in view of Kim US Patent 6100953. Kim (primary reference) teaches all the limitations of claim 17 except a slit formed between adjacent portions of he common electrode. Kim (secondary reference) teaches a slit formed between adjacent portions of the common electrode to enhance the multi-domain effect. Therefore, at the time of the invention it would have been obvious to incorporate slits (recesses) in the primary invention to enhance the multi-domain effect (see secondary reference column 5 lines 62-65).

Conclusion

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phu Vu whose telephone number is (571)-272-1562.

The examiner can normally be reached on 8AM-5PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on (571)-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Phu Vu
Examiner
AU 2871



**KENNETH PARKER
PRIMARY EXAMINER**